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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,141	12/20/2001	Vincent J. Zimmer	10559-632001/ P11183	3533

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EXAMINER	
CHANG, ERIC	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,141	ZIMMER ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,081,890 to Datta, in view of "Extensible Firmware Specification Version 1.02" by Intel Corporation.

4. As to claim 1, Datta discloses a method comprising: initializing a boot routine in a computer [col. 5, lines 29-31]; bootstrapping a volume top file [208] located in a first addressable location [col. 6, lines 27-35] accessible upon the initializing of the boot routine [col. 5, lines 29-31]; and the volume top file bootstrapping a set of firmware modules [col. 5, lines 41-44].

Datta teaches the limitations of the claim, but does not teach that the computer has modular, architecturally defined components for build firmware, wherein the volume top file conforms to an EFI specification.

Intel teaches a method comprising: initializing a boot routine in a computer and bootstrapping a volume top file located in a first addressable location [page 319 paragraph 3], and that firmware modules are subsequently loaded [pages 323-324]. Thus, Intel teaches a boot

method similar to that of Datta. Intel further teaches that the computer and volume top file conform to an EFI architecture [page 319].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the EFI standard as taught by Intel. One of ordinary skill in the art would have been motivated to do so because EFI is a firmware standard, well known to one of ordinary skill in the art, used for booting a computer.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of booting a computer using information from a volume top file to bootstrap additional firmware modules. Moreover, the modular architecturally defined firmware means taught by Intel would improve the flexibility of Datta because it allowed for additional boot order options [page 319, paragraph 1].

5. As to claim 2, Datta discloses using the volume top file to locate a dispatcher module [col. 4, lines 1-14].

6. As to claim 3, Datta discloses using the dispatcher module to access the set of firmware modules [col. 6, lines 36-39].

7. As to claim 4, Datta discloses the set of firmware modules initialize the computer [col. 1, lines 40-46].

8. As to claim 5, Datta discloses using a reset vector to access the volume top file [col. 6, lines 27-35].

9. As to claim 6, Datta discloses the volume top file includes addresses of the set of firmware modules [col. 5, lines 41-49].

10. As to claim 7, Datta discloses the volume top file includes an address of a base of a first firmware module [col. 5, lines 41-49].

11. As to claim 8, Datta discloses the base of the first firmware module includes a boot firmware volume base [col. 3, lines 52-59].

12. As to claim 9, Datta discloses the volume top file comprises an authentication block [col. 3, lines 49-51].

13. As to claim 10, Datta discloses the volume top file validates the set of firmware modules [col. 5, lines 52-56].

14. As to claim 11, Datta discloses designating the volume top file as a last file in the set of firmware modules [col. 6, lines 17-19].

15. As to claim 12, Datta discloses the designating includes aligning an end of the volume top file with a memory boundary [col. 6, lines 17-19 and 27-30].

16. As to claim 13, Datta discloses the memory boundary includes between 4 and 10 giga bytes (Gbyte) of memory [col. 6, lines 27-30].

17. As to claim 14, Datta discloses a system comprising: a non-volatile memory [170] of a computer that initializes a boot routine in the computer [col. 5, lines 29-31]; a processing architecture of the computer configured to bootstrap a volume top file [col. 5, lines 29-31] located in a first addressable location accessible upon the initializing of the boot routine [col. 6, lines 27-35]; and the volume top file configured to bootstrap a set of firmware modules [col. 5, lines 41-44]. Intel further teaches that the computer and volume top file conform to an EFI architecture [page 319].

18. As to claim 15, Datta discloses the volume top file is configured to locate a dispatcher module [col. 4, lines 1-14].

19. As to claim 16, Datta discloses the dispatcher module is configured to access the set of firmware modules [col. 6, lines 36-39].

20. As to claim 17, Datta discloses the set of firmware modules are configured to initialize the computer [col. 1, lines 40-46].

21. As to claim 18, Datta discloses the volume top file includes addresses of the set of firmware modules [col. 5, lines 41-49].

22. As to claim 19, Datta discloses the volume top file includes an address of a base of a first firmware module [col. 5, lines 41-49].

23. As to claim 20, Datta discloses an apparatus comprising: a processor [110]; a non-volatile memory [170] in which is stored: a volume top file [208] located in a first addressable location of the non-volatile memory accessed by a central processing unit (CPU) of a computer, the volume top file being accessible using a reset vector [col. 6, lines 27-35]; a data structure associated with the first firmware module [col. 5, lines 41-51]; and, a second firmware module [204] accessible by the volume top file. Intel further teaches that the computer and volume top file conform to an EFI architecture [page 319].

24. As to claim 21, Datta discloses a first firmware module comprises a distinguished firmware module [col. 5, lines 29-31].

25. As to claim 22, Datta discloses a dispatcher module located by the volume top file [col. 4, lines 1-14].

26. As to claim 23, Datta discloses the set of firmware modules include an initialization routine for initializing the computer [col. 1, lines 40-46].

27. As to claim 24, Datta discloses the volume top file includes an address of a base of the second firmware module [col. 5, lines 41-49].

28. As to claim 25, Datta discloses the base of the second firmware module comprises a boot firmware volume base [col. 3, lines 52-59].

29. As to claim 26, Datta discloses the volume top file includes an authentication block [col. 3, lines 49-51].

30. As to claim 27, Datta discloses the volume top file validates the second firmware module [col. 5, lines 52-56].

31. As to claim 28, Intel discloses the volume top file includes bridges between code that is architecturally specified by the computer and platform code which is not architecturally specified by the computer [page 326 section 17.4.2.2].

32. As to claim 29, Intel discloses locating code and data at fixed locations required by the computer architecture [page 319 paragraph 3].

33. As to claim 30, Intel discloses the volume top file includes a priori information to access a base of firmware system, the firmware base to be used by the set of firmware modules to publish a general set of access services to discover volumes [page 322 paragraph 1].

Response to Arguments

34. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 1, 2006
ec

THUAN N. DU
PRIMARY EXAMINER